WHAT IS CLAIMED IS:

1. A ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix,

wherein plate lines run in the word line direction above the ferroelectric capacitors of memory cells adjacent to each other in the word line direction among the plurality of memory cells,

bit line contacts each for connecting a bit line and an active region of the transistor are placed in regions between the plate lines adjacent to each other in the bit line direction and between the ferroelectric capacitors adjacent to each other in the word line direction,

cut portions are formed at positions of the plate lines near the bit line contacts, and

the active regions of the transistors of the plurality of memory cells extend in directions intersecting with the word line direction and the bit line direction.

2. A ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix,

wherein ferroelectric capacitors of one set of memory cells adjacent to each other in the word line direction among the plurality of memory cells are placed at positions offset

from each other in the bit line direction,

a word line is placed in common for the transistors of the set of memory cells,

a plate line is placed in common for the ferroelectric capacitors of the set of memory cells, and

bit line contacts each for connecting a bit line and an active region of the transistor are placed between the plate lines adjacent to each other in a bit line direction.

3. A ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix,

wherein ferroelectric capacitors of one set of memory cells adjacent to each other in the word line direction among the plurality of memory cells are placed at positions offset from each other in the bit line direction,

a word line is placed in common for the transistors of the set of memory cells,

plate lines are placed separately for the respective ferroelectric capacitors of the set of memory cells, and

bit line contacts each for connecting a bit line and an active region of the transistor are placed between plate line groups each composed of the plurality of plate lines corresponding to the set of memory cells.

4. A ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix,

wherein ferroelectric capacitors of one set of memory cells adjacent to each other in the word line direction among the plurality of memory cells are placed at positions offset from each other in the bit line direction,

a plate line is placed in common for the ferroelectric capacitors of the set of memory cells, and

bit line contacts each for connecting a bit line and an active region of the transistor are placed on both sides of the plate line in the bit line direction.

5. A ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix,

wherein active regions of the transistors of the plurality of memory cells extend through between the ferroelectric capacitors in the bit line direction, and

word lines include: gate electrodes having a relatively large width formed above portions of the active regions extending through between the ferroelectric capacitors in the bit line direction; and interconnections of the ferroelectric capacitors having a relatively small width and extending in the bit line direction.

6. The ferroelectric memory according to claim 5, wherein the active regions have a bent shape.

7. A ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix,

wherein ferroelectric capacitors adjacent to each other in the bit line direction with a bit line contact therebetween among a plurality of ferroelectric capacitors constituting the plurality of memory cells are placed not to be offset from each other in the word line direction, while ferroelectric capacitors adjacent to each other in the bit line direction without a bit line contact therebetween among a plurality of ferroelectric capacitors constituting the plurality of memory cells are placed at positions offset from each other in the word line direction,

active regions of the transistors of the plurality of memory cells extend through in the bit line direction between the ferroelectric capacitors adjacent to each other in the word line direction, and

word lines include: gate electrodes having a relatively large width formed above the active regions; and interconnections of the ferroelectric capacitors having a relatively small width and extending in the bit line

direction.

8. A ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix,

wherein ferroelectric capacitors of a pair of memory cells adjacent to each other in the word line direction among the plurality of memory cells are placed at positions offset from each other in the bit line direction,

a plate line is placed in common for the ferroelectric capacitors of the pair of memory cells, and

a word line is placed in common for the transistors of the pair of memory cells and formed between the ferroelectric capacitors of the pair of memory cells.

9. A ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix,

wherein ferroelectric capacitors of pairs of memory cells adjacent to each other in the word line direction among the plurality of memory cells are placed at positions offset from each other in the bit line direction,

active regions of the transistors of ones of the pairs of memory cells extend through between the ferroelectric capacitors of the others of the pairs of memory cells in the

bit line direction, intersecting with a plate line for the other memory cells,

first word lines are provided for the transistors of the ones of the pairs of memory cells, while second word lines are provided for the transistors of the other memory cells, and

the second word lines are narrowed at portions intersecting with the active regions of the transistors of the ones of the pairs of memory cells to a degree that the active regions are prevented from being turned to an OFF state.

10. A ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix,

wherein bit lines are composed of active regions running through in the bit line direction between the ferroelectric capacitors of pairs of memory cells adjacent to each other in the word line direction among the plurality of memory cells, and provided integrally with active regions of the transistors of the plurality of memory cells, and

word lines include: interconnections having a small width formed above the bit lines to prevent the bit lines from being turned to an OFF state; and gate electrodes having a width larger than the interconnections formed above the

active regions of the transistors.